CLAIMS

What is claimed is:

1. A method for generating a set of clock signals in a system, the set of clock signals comprising a set of sampling clock signals, the system comprising a set of subsystems, each of the subsystems comprising an analog section, each of the analog sections operating in accordance with a corresponding one of the sampling clock signals, the method comprising the operations of:

(a) generating a phase error for each of the sampling clock signals from a corresponding phase detector;

(b) inputting each of the phase errors to a corresponding loop filter;

(c) generating filtered phase errors from the corresponding loop filters;

(d) inputting each of the filtered phase errors to a corresponding oscillator;

(e) generating phase control signals from the corresponding oscillators;

(f) inputting each of the phase control signals to a corresponding phase selector; and

(g) generating the sampling clock signals from the corresponding phase selectors.

2. The method of claim 1 wherein the set of clock signals further comprises a receive clock signal and wherein each of the subsystems further comprises a digital section, the digital sections operating in accordance with the receive clock signal.

3. The method of claim 2 wherein the receive clock signal is related to one of the sampling clock signals.

4. The method of claim 3 further comprising the operations of:

(1) combining one of the phase control signals with a receive clock offset to produce a phase shift value;

(2) inputting the phase shift value to a receive clock phase selector; and

(3) generating the receive clock signal from the receive clock phase selector.

5. The method of claim 4 wherein the phase shift value comprises a set of phase steps and wherein operation (2) comprises the operation of inputting one phase step of the phase shift value at a time to the receive clock phase selector.

6. The method of claim 1 wherein the set of clock signals further comprises a transmit clock signal and wherein each of the subsystems further comprises a transmit section, the transmit sections operating in accordance with the transmit clock signal.

7. The method of claim 6 further comprising the operations of:

inputting a transmit clock offset to a transmit clock phase selector; and

generating the transmit clock signal from the transmit clock phase selector.

8. The method of claim 7 wherein the transmit clock offset is equal to zero.

9. The method of claim 6 wherein the transmit clock signal is related to one of the sampling clock signals.

10. The method of claim 9 further comprising the operations of:

inputting one of the phase control signals to a transmit clock phase selector; and

generating the transmit clock signal from the transmit clock phase selector.

11. The method of claim 1 wherein each of the phase detectors receives a corresponding slicer error and a corresponding tentative decision from a decoding system.

12. The method of claim 11 wherein operation (a) comprises:

(1) generating a pre-cursor phase error by multiplying the corresponding tentative decision by a delayed version of the corresponding slicer error;

(2) generating a post-cursor phase error by multiplying the corresponding slicer error by a delayed version of the corresponding tentative decision;

(3) combining the pre-cursor and post-cursor phase errors to produce the corresponding phase error.

13. The method of claim 12 wherein operations (1), (2) and (3) are performed via a lattice structure, the lattice structure comprising two delay elements, two multipliers and an adder.

14. The method of claim 12 wherein operation (3) includes the operation of combining the pre-cursor, post-cursor phase errors and an offset input from a control unit to produce the corresponding phase error.

15. The method of claim 1 wherein operation (c) comprises:

(1) accumulating a number of consecutive values of one of the phase errors via a first filter, resulting in a sum value;

(2) outputting the sum value from the first filter;

(3) integrating the sum value via a second filter to produce an integral value; and

(4) combining the sum value and the integral value to produce a filtered phase error.

16. The method of claim 15 wherein operation (3) includes the operation of scaling the integrated sum value by a scale factor to produce the integral value.

17. The method of claim 15 wherein operation (c) further comprises, before operation (3), the operation of multiplying the sum value by a factor different than 1 when the system is operating in a different bandwidth mode.

18. The method of claim 1 wherein operation (e) comprises the operation of filtering recursively the filtered phase errors to produce the corresponding phase control signals.

19. The method of claim 18 wherein operation (e) further comprises the operation of scaling, before filtering recursively, the filtered phase errors by a scale factor.

20. The method of claim 1 wherein operation (g) comprises the operations of:

(1) inputting a multi-phase input signal from a clock generator to each of the phase selectors; and

(2) selecting at each of the phase selectors one of the phases of the multi-phase input signal based on the phase control signal received from the corresponding oscillator.

21. A timing recovery system for generating a set of clock signals in a processing system, the set of clock signals comprising a set of sampling clock signals, the processing system comprising a set of processing subsystems, each of the processing subsystems comprising an analog section, each of the analog sections

operating in accordance with a corresponding one of the sampling clock signals, the timing recovery system comprising:

(a) a set of phase detectors generating phase errors for the corresponding sampling clock signals;

(b) a set of loop filters coupled to the corresponding phase detectors, the loop filters receiving the corresponding phase errors and generating filtered phase errors;

(c) a set of oscillators coupled to the corresponding loop filters, the oscillators receiving the filtered phase errors and generating phase control signals; and

(d) a set of phase selectors coupled to the corresponding oscillators, the phase selectors receiving the phase control signals and generating the sampling clock signals.

22. The timing recovery system of claim 21 wherein the set of clock signals further comprises a receive clock signal and wherein each of the processing subsystems further comprises a digital section, the digital sections operating in accordance with the receive clock signal.

23. The timing recovery system of claim 22 wherein the receive clock signal is related to one of the sampling clock signals.

24. The timing recovery system of claim 23 further comprising a first adder and a receive clock phase selector, the first adder receiving one of the phase control signals and a receive clock offset and generating a phase shift value, the receive clock phase selector receiving the phase shift value and generating the receive clock signal.

25. The timing recovery system of claim 24 wherein the phase shift value comprises a set of phase steps and wherein the receive clock phase selector receives the phase shift value in the form of consecutive phase steps.

26. The timing recovery system of claim 21 wherein the set of clock signals further comprises a transmit clock signal and wherein each of the subsystems further comprises a transmit section, the transmit sections operating in accordance with the transmit clock signal.

27. The timing recovery system of claim 26 further comprising a transmit clock phase selector, the transmit clock phase selector receiving a transmit clock offset and generating the transmit clock signal.

28. The timing recovery system of claim 27 wherein the transmit clock offset is equal to zero.

29. The timing recovery system of claim 26 wherein the transmit clock signal is related to one of the sampling clock signals.

30. The timing recovery system of claim 29 further comprising a transmit clock phase selector, the transmit clock phase selector receiving one of the phase control signals and generating the transmit clock signal.

31. The timing recovery system of claim 21 wherein each of the phase detectors receives a corresponding slicer error and a corresponding tentative decision from a decoding system.

32. The timing recovery system of claim 31 wherein each of the phase detectors comprises a lattice structure, the lattice structure comprising two delay elements, two multipliers and an adder, the lattice structure generating a pre-cursor phase error by multiplying the corresponding tentative decision by a delayed version of the corresponding slicer error and generating a post-cursor phase error by multiplying the corresponding slicer error by a delayed version of the corresponding

tentative decision and combining the pre-cursor and post-cursor phase errors to produce the corresponding phase error.

33. The timing recovery system of claim 32 wherein at least one of the phase detectors further receives an offset input from a control unit and wherein the associated lattice structure combines the pre-cursor, post-cursor phase errors and the offset input to produce the corresponding phase error.

34. The timing recovery system of claim 21 wherein at least one of the loop filters comprises a first filter for accumulating a number of consecutive values of one of the phase errors to produce a filtered phase error.

35. The timing recovery system of claim 21 wherein at least one of the loop filters comprises a first filter for accumulating a number of consecutive values of one of the phase errors to produce a sum value, a second filter for integrating the sum value to produce an integral value and an adder for combining the sum value and the integral value to produce a filtered phase error.

36. The timing recovery system of claim 35 wherein the second filter includes a multiplier for scaling the integrated sum value by a scale factor to produce the integral value.

37. The timing recovery system of claim 35 wherein at least one of the loop filters further comprises a multiplier for multiplying the sum value by a factor different than 1 when the system is operating in a different bandwidth mode.

38. The timing recovery system of claim 21 wherein each of the oscillators comprises an infinite impulse response filter for filtering recursively the filtered phase errors to produce the corresponding phase control signals.

39. The timing recovery system of claim 38 wherein at least one of the oscillators further comprises a multiplier for scaling the filtered phase errors by a

scale factor and outputting the scaled filtered phase errors to the associated impulse response filter.

40. The timing recovery system of claim 21 wherein each of the phase selectors receives a multi-phase input signal from a clock generator and selects one of the phases of the multi-phase input signal based on the phase control signal received from the corresponding oscillator.

41. A timing recovery system for generating a set of clock signals in a processing system, the set of clock signals comprising a set of sampling clock signals, the processing system comprising a set of processing subsystems, each of the processing subsystems comprising an analog section, each of the analog sections operating in accordance with a corresponding one of the sampling clock signals, the timing recovery system comprising:

(a) a set of phase detectors generating phase errors for the corresponding sampling clock signals;

(b) a set of loop filters coupled to the corresponding phase detectors, the loop filters receiving the corresponding phase errors and generating filtered phase errors;

(c) a set of digital-to-analog (D/A) converters coupled to the loop filters, the D/A converters receiving the filtered phase errors and generating analog filtered phase errors; and

(d) a set of oscillators coupled to the corresponding D/A converters, the oscillators receiving the analog filtered phase errors and generating the sampling clock signals.

42. The timing recovery system of claim 41 wherein the oscillators comprise varactor diodes.